REMARK

In the Office Action, claims 1-40 were pending of which claims 8-26 and 34-40 were withdrawn. In this response, claims 8-26 and 34-40 have been canceled without prejudice. Claims 1 and 27 have been amended. New claims 41-58 have been added. Thus, claims 1-7, 27-33, and 41-58 remain pending. No new matter has been added. Reconsideration of the present application as amended is respectfully requested.

Claims 1-5 and 27-31 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,862,280 of Bertagna ("Bertagna") in view of U.S. Patent No. 6,678,248 of Haddock et al. ("Haddock"). Claims 5 and 31 were rejected under 35 U.S.C. 103(a) as being unpatentable over Bertagna in view of Haddock and U.S. Patent No. 6,717,951 of Stanton et al. ("Stanton"). The statuses of claims 32-33 are unclear. Applicant hereby reserves the right to swear behind the above-cited references.

In view of the foregoing amendments, it is respectfully submitted that claims 1-7, 27-33, and 41-58 as amended include limitations that are not disclosed or suggested by the cited references, individually or in combination. Specifically, independent claim 1 recites as follows:

> 1. A method for controlling admittance of a data packet into a memory buffer, the method comprising:
> performing, prior to queuing the data packet for routing by a processor, the following:
> receiving a data packet from one of at least two different ports;
> determining a priority value within the data packet;
> determining an admittance group identifier for the data packet based on the priority value and the port the data packet was received; and
> admitting the data packet into the memory buffer associated with a group identified by the determined admittance group identifier; and
> queuing the data packet from the memory buffer to one of a number of queues for routing by the processor upon determining that a number of data packets stored in the memory buffer and having the admittance group identifier is not greater than a threshold value associated with the determined admittance group identifier.

(Emphasis added)

Independent claim 1 includes limitations of prior to queuing a data packet to a queue for routing by a processor, determining a priority of the data packet to determine an admittance group identifier for identifying a group from which the data packet belongs, admitting the data packet into the memory buffer associated with a group identified by the admittance group identifier, and queuing the data packets of the group into one of the queues only if the number of the data packets within the group would not exceed a predetermined threshold value associated with the group. Thereafter the processor can perform routing on the queued data packets. It is respectfully submitted that the above limitations are absent from the cited references.

Rather, Bertagna is related to how to prioritize data packets (see, Abstract of Bertagna). Specifically, Bertagna is based on an assumption that "[t]here is no provision in the standard, however, to use other values in determining the outbound tag priority. It may be desirable to determine an outbound tag priority based on values other than the inbound tag priority and the receiving physical port" (see col. 1, lines 27 to 32 of Bertagna).

In contrast, the present invention as claimed is related to an admittance process for admitting a data packet into a memory buffer before queuing the data packet for routing by a processor. There is no disclosure within Bertagna for such a process, particularly before queuing a data packet for routing by a processor.

It appears that a switching engine 211 (e.g., a processor) of Bertagna performs determining the outbound priority of packets based on inbound tagged priority of the packets and routing the packets, while the data packets are stored or queued within the switch engine. Specifically, Bertagna stated:

> "Controller 201 receives packets off LANs, formats them and transmits them to engine 211. Controller 201 also receives packets from engine 211, formats them and transmits them on LANs. Engine 211 is coupled to Elements for facilitating priority processing, including virtual trunk finder 221, priority remap database 231, content-addressable memory (CAM) 241, forwarding database 251 and queue remap database 261. Particularly, engine 211 receives packets from controller 201, subjects them to ingress priority processing and transmits them on the one of buses 111-119 for which interface 200 is the root. Engine 211 also receives packets from buses 111-119, subjects selected ones of them to egress priority processing and transmits selected ones of them to controller 201. Ingress priority processing is conducted with the assistance of virtual trunk finder 221, priority remap database 231, CAM 241 and forwarding database 251, while egress priority processing is conducted with the assistance of CAM 241, forwarding database 251 and queue remap database 261."

(Figs. 1-2, col. 3, lines 44 to 67 of Bertagna, emphasis added).

Bertagna further stated:

> "At switching engine 211, packet 400 is subjected to ingress priority processing to prepare packet 400 for transmission on the bus for which interface 200 is the root. Engine 211 identifies packet 400 as a tagged packet by reference to CTRL. Once identified, engine 211 strips PORT, CTRL and TAG2 and TAG 3 (including the twelve-bit VLAN identifier therein) from packet 400."

(Figs. 2 and 4, col. 4, lines 37 to 51 of Bertagna, emphasis added).

As set forth above, the data packets of Bertagna are stored or queued within the switch engine and routed by the switch engine. There is no admittance process into a memory buffer based on the priorities of the data packets prior to the switching engine transmitting the data onto the buses (e.g., routing the data packets).

In addition, independent claim 1 requires that only the data packets of a group having a number of data packets that does not exceed a threshold associated with the group are queued in a queue for routing by a processor. Extra data packets belonging to the same group will be discarded. It is respectfully submitted that these limitations are also absent from Bertagna.

Similarly, although Haddock and Stanton are related to setting priority of network data packets, Haddock and Stanton fail to disclose the admittance process set forth above, particularly, prior to queuing the data packets for a processor to process the data packets for routing.

In addition, there is no suggestion within Bertagna, Haddock, and Stanton to combine with each other. Such a combination can only be found based on the impermissible hindsight of Applicant's own disclosure. Even if they were combined, such a combination still lacks the limitations set forth above. Therefore, for the reasons discussed above, it is respectfully submitted that independent claim 1 is patentable over the cited references.

Similarly, independent claims 27 and 57-58 include limitations similar to those recited in claim 1. Thus, for at least the reasons similar to those discussed above, independent claims 27 and 57-58 are patentable over the cited references.

Given that the rest of the claims depend from one of the above independent claims, at least for the reasons similar to those discussed above, it is respectfully submitted that the rest of the claims are patentable over the cited references. Withdrawal of the rejections is respectfully requested.

In view of the foregoing, Applicant respectfully submits the present application is now in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call the undersigned attorney at (408) 720-8300.

Please charge Deposit Account No. 02-2666 for any shortage of fees in connection with this ıesponse.

Respectfully submitted,

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